REMARKS

Reconsideration of this application as amended is respectfully requested.

Claims 1-23, 32-34, and 38-43 are pending in the application. Claims 1-23, 32-34, and 38-43 are rejected.

Claims 1, 3, 5-6, 8-10, and 32-34 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants' Admitted Prior Art ("APA") in view of U.S. Patent No. 6,229,737 of Walukas et al. ("Walukas"). Claims 2, 4, 7, and 11-23 stand rejected under 35 U.S.C §103(a) as being unpatentable over APA in view of Walukas and further in view of U.S. Patent No. 5,966,723 of James et al. ("James"). Claims 38-40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of James. Claims 41-43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of James and further in view of Walukas.

Claims 1, 7, 9-10, 12, 18-19, 32, and 38 have been amended.

The drawings is objected to for having an enlarged view not labeled separately or properly. Figure 3 has been amended with labels **310, 320, 330**. Applicants respectfully submit that the objections have been overcome.

Claims 1, 3, 5-6, 8-10, and 32-34 are rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants' admitted prior art (APA) in view of Walukas. Applicants respectfully submit that Claims 1-23, 32-34, and 38-43 are patentable under 35 U.S.C. §103(a) over APA in view of Walukas.

A prima facie case of obviousness exists when (1) either the reference themselves or the knowledge generally available to one of ordinary skill in the art contain some suggestion or motivation to modify the reference or to combing the reference teachings; (2) a reasonable expectation of success exist; and (3) the prior art reference or references teach or suggest all the claim limitations.

Here, neither APA nor Walukas, individually or in combination, teach or suggest the present claims. It is respectfully submitted that APA and Walukas do not teach or suggest a combination with each other. The Examiner has generally referred to pages 1-4 and Figures 1-2 of the patent application as Admitted Prior Art. Applicants submit that the APA discloses a program command sequence including sending a 'Program Set-Up'

command and then sending the program address and program data. The 'Program Set-Up' commands sets the Command User Interface (CUI) into a state such that the next write will load the address and data registers. Furthermore, if there are more addresses to program after the first address, steps 110, including the program set up, through 150 have to be repeated. (see e.g., page 2, line 11 to page 3, line 7).

The timing diagram also shows that the device is set up for programming at T4 with the program command on the data bus and the program address on the address bus. The actual program occurs when the program address and program data are sent at time T5. The control logic uses the program address 222 and the program data to program the appropriate address in the memory array at T6. Furthermore, lines 15-18 explicitly state that:

> Each program needs to have the program setup in order to program
> an address. Hence, when more than one address location needs to
> be programmed, the program setup has to be repeated for each
> program operation.

(see e.g., page 3, line 17 to page 4, line 19). Thus, the APA discloses sending a program command *each and every time* a program operation to an address is performed.

Walukas discloses a method and apparatus for interleaving flash memory programming with E^2ROM memory programming. The algorithm starts with initialization of points that point to memory locations at which data is to be stored in the respective devices. An end flag is asserted when the last memory location has been programmed. The processor polls the flash and writes a page of data to the flash memory at the location designated by the F pointer if the flash is not busy. If the flash is busy, the processor re-polls. Following the information download to the flash internal buffer, the processor attempts to download information to the E^2ROM. If the E^2ROM is not busy, the processor downloads a page of data to the E^2ROM at the location designated by the E pointer. The processor continues to download data to both devices until all has been programmed. (see e.g. col. 5, lines 1-63). Thus Applicants submit that Walukas discloses an interleaving algorithm wherein an E^2ROM programming cycle is performed while the flash memory is programming its memory array.

In any event, even if APA and Walukas were combined, such a combination

would lack one or more features of Claim 1. A combination of APA and Walukas would fail to teach or disclose:

> sending a command to a memory device, said command requesting said memory device to enter a fast program mode;
> sending a first address to said memory device;
> sending a first packet of data to said memory device, said first packet of data to be programmed at said first address;
> sending a first write signal to said memory device, said first write signal to cause said first packet of data to be programmed at said first address;
> sending a second packet of data to said memory device; and
> sending a second write signal to said memory device, said second write signal to cause said second packet of data to be programmed at a second address, said second address generated by said memory device by incrementing said first address a predetermined amount.

(Claim 1).

Therefore the combination of APA and Walukas fails to teach or disclose that claimed in Claim 1. Furthermore, for at least the same reasons noted above with respect to Claim 1, Claims 2-23, 32-34, and 38-43 are similarly distinguished over the APA and Walukas reference, alone or in combination.

Claims 2, 4, 7, and 11-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of Walukas and further in view of James. Claims 2, 4, 7, and 11 depend directly or indirectly from independent base Claim 1 and add additional limitations. Applicants respectfully submit that Claims 1-23, 32-34, and 38-43 are patentable under 35 U.S.C. §103(a) over APA in view of Walukas and further in view of James.

Applicants submit that neither APA nor Walukas nor James, individually or in combination, teach or suggest the present claims. It is respectfully submitted that APA, Walukas, and James do not teach or suggest a combination with each other. APA discloses a program command sequence including sending a 'Program Set-Up' command and then sending the program address and program data as discussed above. Walukas discloses a method and apparatus for interleaving flash memory programming with E^2ROM memory programming as discussed above. (see e.g., col. 5, lines 1-63).

James discloses a method and apparatus for a serial programming mode for non-volatile memory. James discloses having to only toggle signals at a clock input and a serial data input of the flash device during programming operations. When a FSI# signal is asserts, the serial interface mode is entered. Data pin DQ15 serves as a serial data output SDO. Data pin DQ0 serves as a serial data input SDI. Address pin A15 serves as a serial clock input SCLK to shift data from the DQ0/SDI input through either the command/address shift register 17 or the data register 15. Once serial interface mode has been enabled, data from SDI is shifted into a control bit storage element 14 at each rising edge of serial clock signal SCLK. Also, at each rising edge of SCLK, the bit stored in the control bit storage element is shifted into either command/address shift register or data shift register. Whether input bits are shifted to the command/address shift register or data register is determined by device state machine based on a control bit shifted into control bit storage element. James disclose that if the control bit is zero, the next sixteen input bits are shifted into data shift register. If the control bit is nonzero then the next eight input bits are shifted into command/address shift register. (see e.g., col. 4, line 51 to col. 5, line 40).

However, James also discloses that the control bit is evaluated at numerous occasions to determine what to do. For example, the control bit is evaluated at block 52 to determine if another address byte is received. If the control bit is zero, then the starting address is fully specified. If the control bit is nonzero, then more address bits are forthcoming. (see e.g., col. 8, lines 1-33). The control bit is again evaluated at block 65 to determine whether the data shift state is entered. If the control bit is nonzero, then the command shift state is entered to receive a new command. At decision block 32, the control bit is evaluated to determine whether the command in the command register is executed at the falling edge of the serial clock immediately following entry into data shift state. A program, erase, or read-status operation can be entered. (see e.g., col. 8, line 34-50).

Furthermore, James discloses at col. 9, lines 52-57, that:

> A control bit follows each data word, and because the command
> register now contains a PROGRAM command, the data word is
> transferred from the data shift register to the device data register at

the falling edge of the serial clock which follows receipt of a zero-valued control bit.

A control bit is appended to the data word shifted into the flash memory device during step 121 as the next data word is shifted in. Depending on the write status of the previous write operation, a zero-value control bit can be shifted into the flash memory to cause the new data word to be shifted into the shift register for programming if the status is successful. (see e.g., col. 10, lines 7-26). James also discloses that:

> Eventually the device should complete the previous write operation and indicate that it is no longer busy. If the *previous write operation* is detected to have been successfully completed, then a *program command* is shifted into the command/address shift register at step 131, followed by a *zero-valued control bit* to indicate that the next sequence of bits is to be a data word.

(see e.g., Figure 4 and col. 11, lines 9-30 with emphasis). Thus James sends a program command and a control bit for each program.

In any event, even if APA, Walukas, and James were combined, such a combination would lack one or more features of Claim 1. A combination of APA, Walukas, and James would fail to teach or disclose:

> sending a command to a memory device, said command requesting said memory device to enter a fast program mode;
> sending a first address to said memory device;
> sending a first packet of data to said memory device, said first packet of data to be programmed at said first address;
> sending a first write signal to said memory device, said first write signal to cause said first packet of data to be programmed at said first address;
> sending a second packet of data to said memory device; and
> sending a second write signal to said memory device, said second write signal to cause said second packet of data to be programmed at a second address, said second address generated by said memory device by incrementing said first address a predetermined amount.

(Claim 1).

Therefore the combination of APA, Walukas, and James fails to teach or disclose that claimed in Claim 1. Furthermore, for at least the same reasons noted above with respect to Claim 1, Claims 2-23, 32-34, and 38-43 are similarly distinguished over the

APA, Walukas, and James references, alone or in combination.

Claims 38-40 are rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of James. Applicants respectfully submit that Claims 1-23, 32-34, and 38-43 are patentable under 35 U.S.C. §103(a) over APA in view of James.

Applicants submit that neither APA nor James, individually or in combination, teach or suggest the present claims. It is respectfully submitted that APA and James do not teach or suggest a combination with each other. APA discloses a program command sequence including sending a 'Program Set-Up' command and then sending the program address and program data as discussed above. James discloses a method and apparatus for a serial programming mode for non-volatile memory as discussed above.

In any event, even if APA and James were combined, such a combination would lack one or more features of Claim 38. A combination of APA and James would fail to teach or disclose:

> receiving a command to enter a fast program mode to program a first piece of data at a first address;
> entering into said fast program mode;
> programming said first piece of data at said first address in response to a write signal;
> checking whether termination of said fast program mode is indicated or if a second piece of data is to be written, wherein said checking further comprises detecting if an incoming address is different from said first address;
> exiting said fast program mode if said termination of said fast program mode is indicated, else incrementing said first address to a second address; and
> programming said second piece of data at said second address in response to another write signal.

(Claim 38).

Therefore the combination of APA and James fails to teach or disclose that claimed in Claim 38. Furthermore, for at least the same reasons noted above with respect to Claim 38, Claims 1-23, 32-34, and 39-43 are similarly distinguished over the APA and James references, alone or in combination.

Claims 41-43 are rejected under 35 U.S.C. §103(a) as being unpatentable over APA in view of James and further in view of Walukas. Claims 41-43 depend directly

from independent base Claim 38 and add additional limitations. Applicants respectfully submit that Claims 1-23, 32-34, and 38-43 are patentable under 35 U.S.C. §103(a) over APA in view of James and further in view of Walukas.

Applicants submit that neither APA nor James nor Walukas, individually or in combination, teach or suggest the present claims. It is respectfully submitted that APA, James, and Walukas do not teach or suggest a combination with each other. APA discloses a program command sequence including sending a 'Program Set-Up' command and then sending the program address and program data as discussed above. James discloses a method and apparatus for a serial programming mode for non-volatile memory as discussed above. Walukas discloses a method and apparatus for interleaving flash memory programming with E^2ROM memory programming as discussed above.

In any event, even if APA, James, and Walukas were combined, such a combination would lack one or more features of Claim 38. A combination of APA, James, and Walukas would fail to teach or disclose:

> receiving a command to enter a fast program mode to program a first piece of data at a first address;
> entering into said fast program mode;
> programming said first piece of data at said first address in response to a write signal;
> checking whether termination of said fast program mode is indicated or if a second piece of data is to be written, wherein said checking further comprises detecting if an incoming address is different from said first address;
> exiting said fast program mode if said termination of said fast program mode is indicated, else incrementing said first address to a second address; and
> programming said second piece of data at said second address in response to another write signal.

(Claim 38).

Therefore the combination of APA, James, and Walukas fails to teach or disclose that claimed in Claim 38. Furthermore, for at least the same reasons noted above with respect to Claim 38, Claims 1-23, 32-34, and 39-43 are similarly distinguished over the APA, James, and Walukas references, alone or in combination.

Claim amendments, other than those specifically discussed above, were

voluntarily made to broaden the scope of the Claims.

In summary, for the reasons noted above, Claims 1-23, 32-34, and 38-43 are distinguished over the cited art and are in condition for allowance. It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. Favorable action is respectfully solicited. Allowance of the Claims is respectfully requested.

The Examiner is invited to call the undersigned at 408-765-8648 if there remains any issue with allowance of this case.

Please charge any additional charges to our Deposit Account No. 02-2666.

Respectfully submitted,

Dated: 6/25, 2003
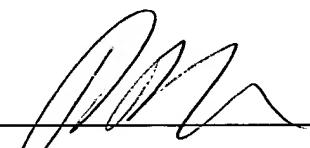
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